

FIG 1

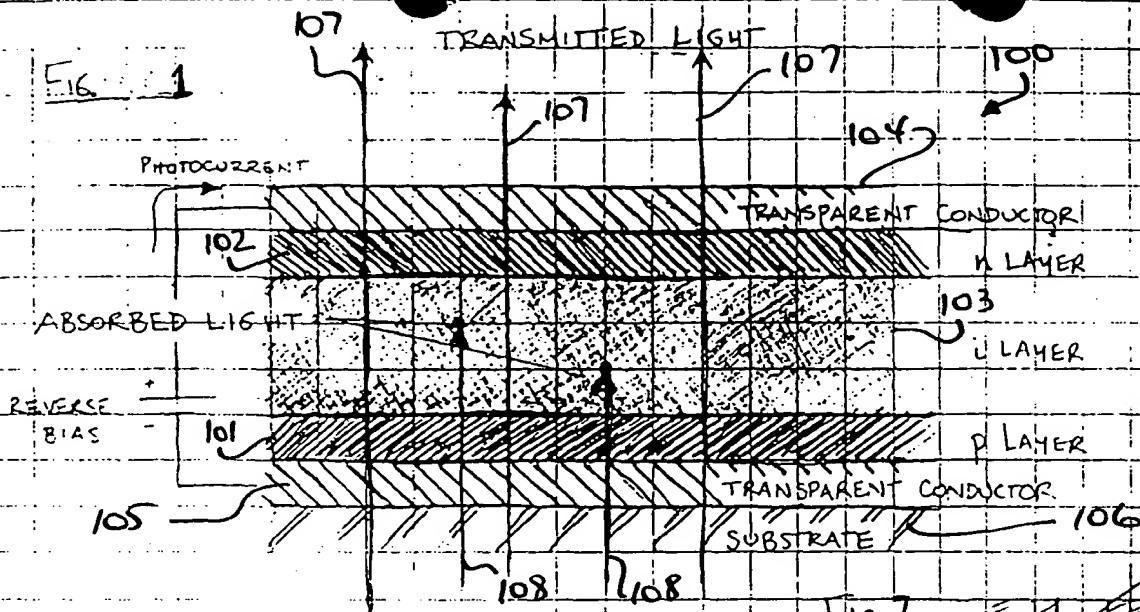


FIG 4

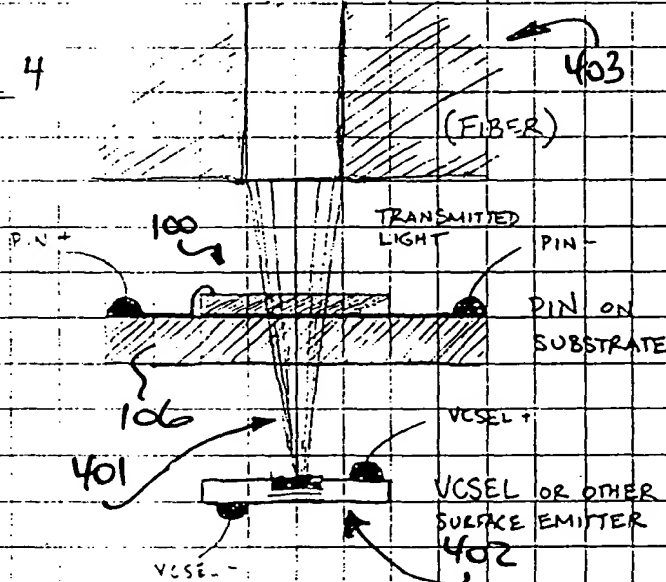


FIG 7

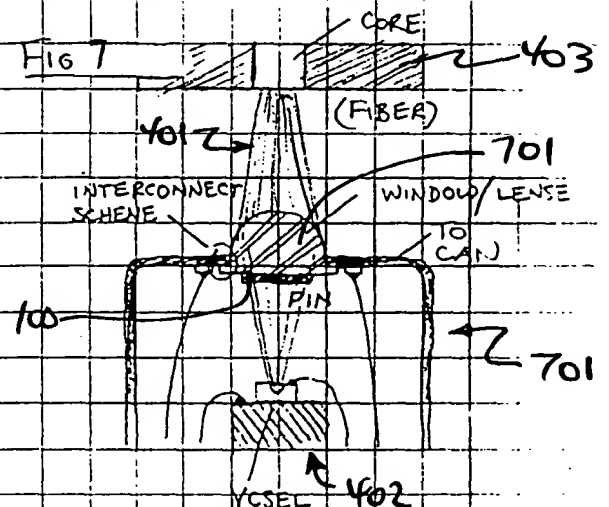


FIG 5

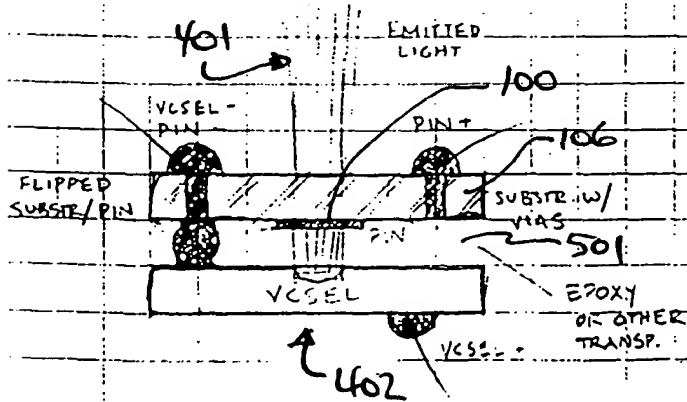
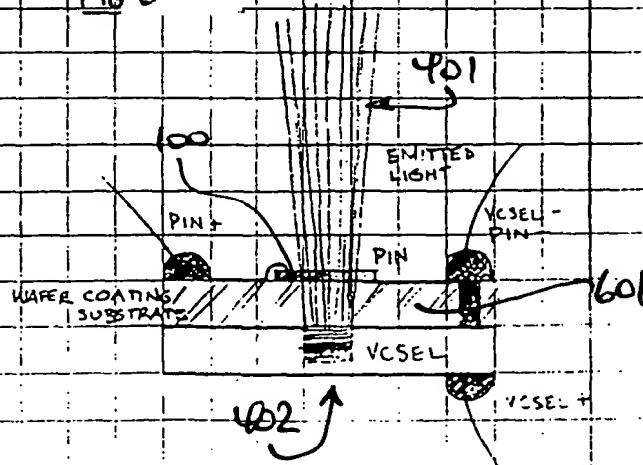


FIG 6



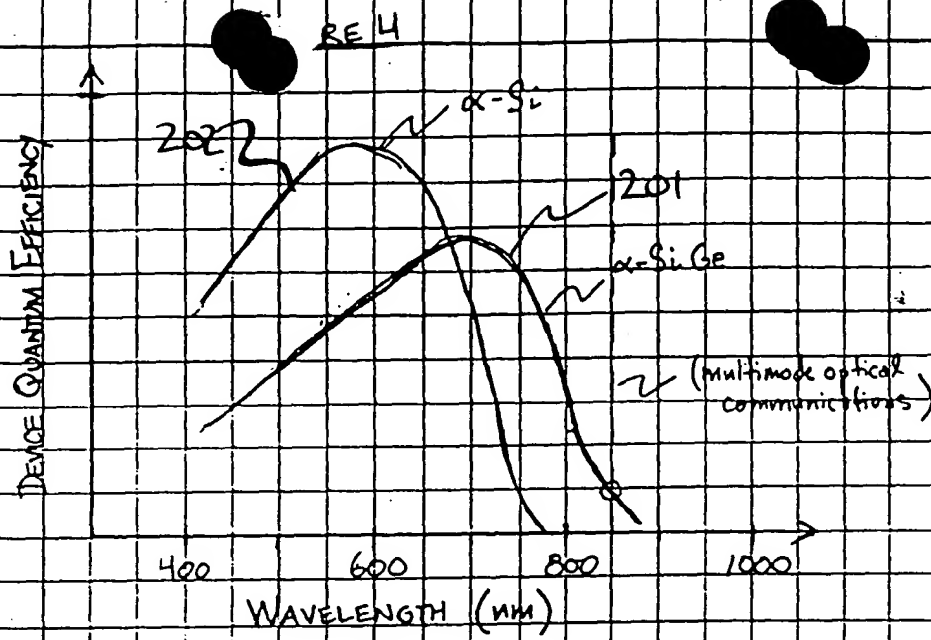


Fig. 2.

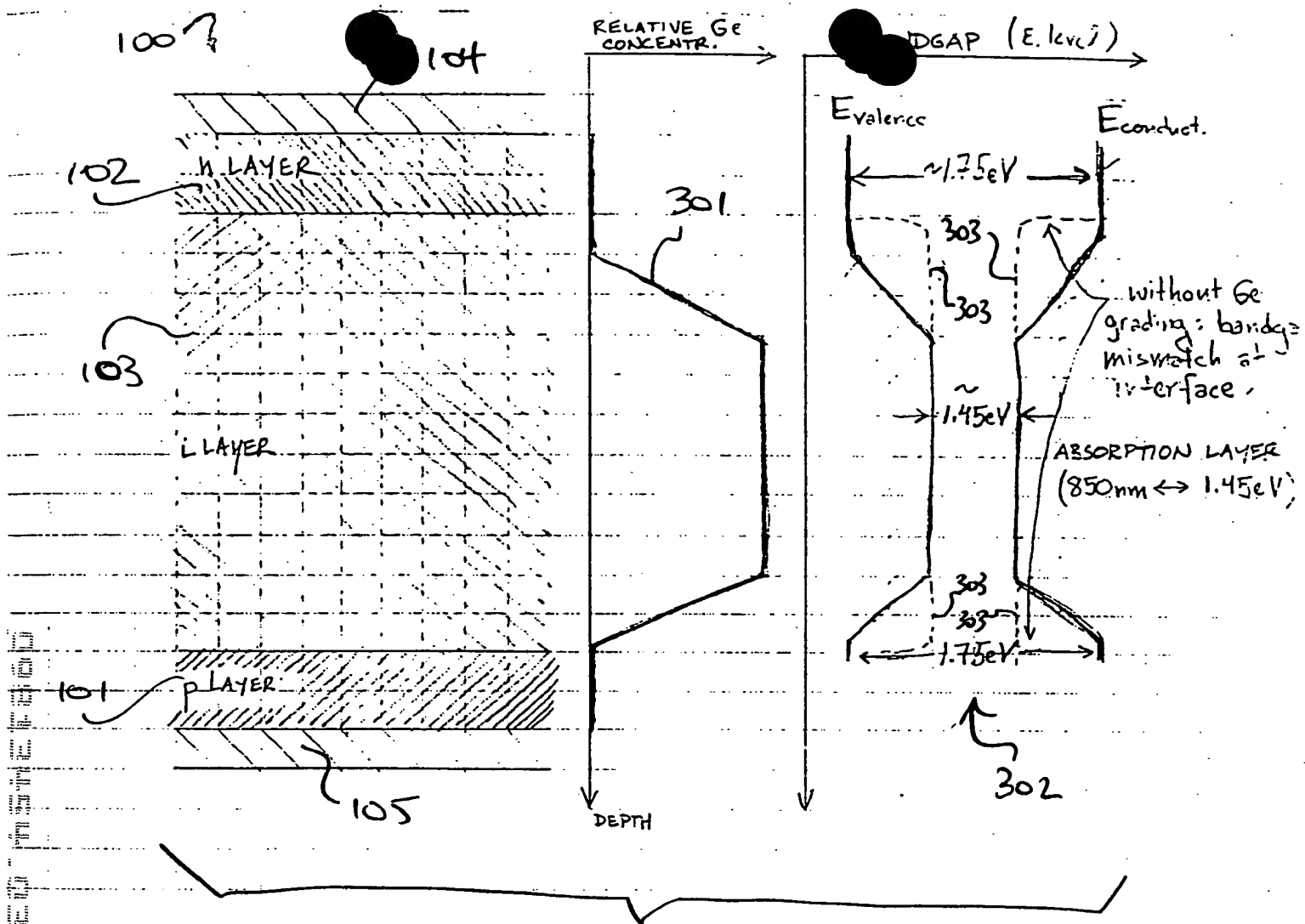


Fig. 3

80
REN
OR

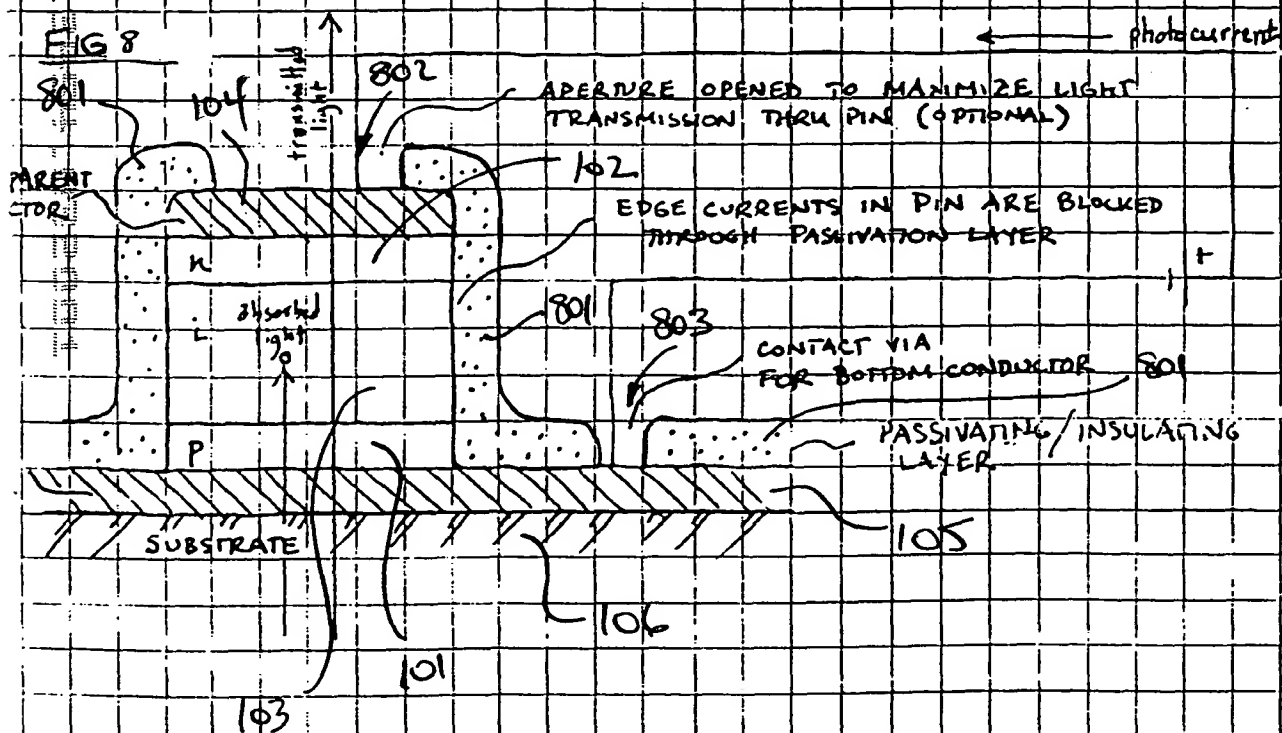
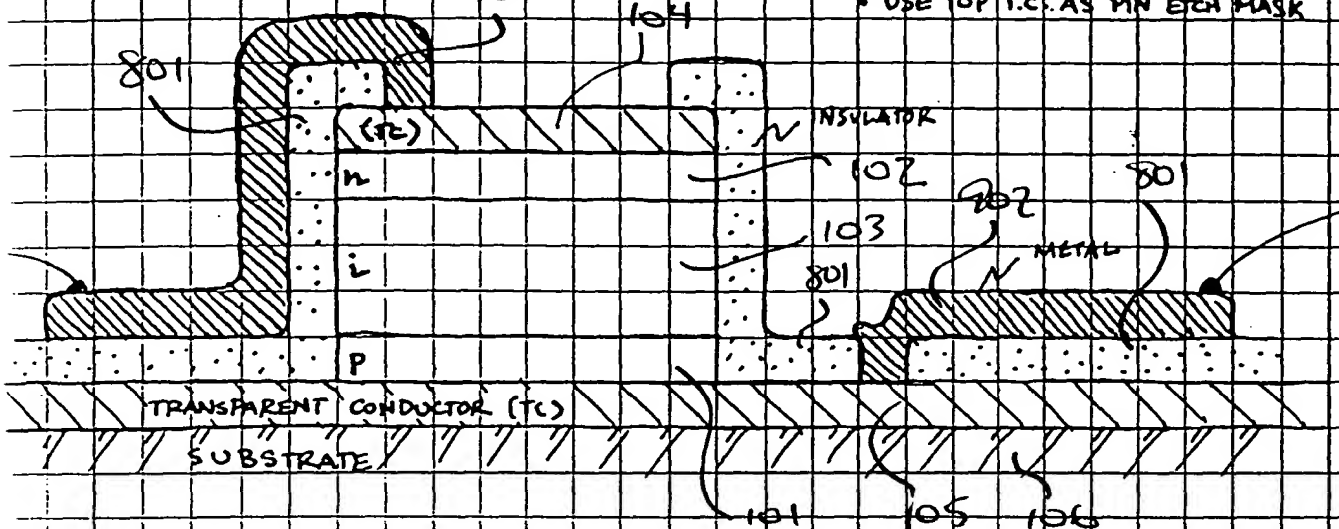
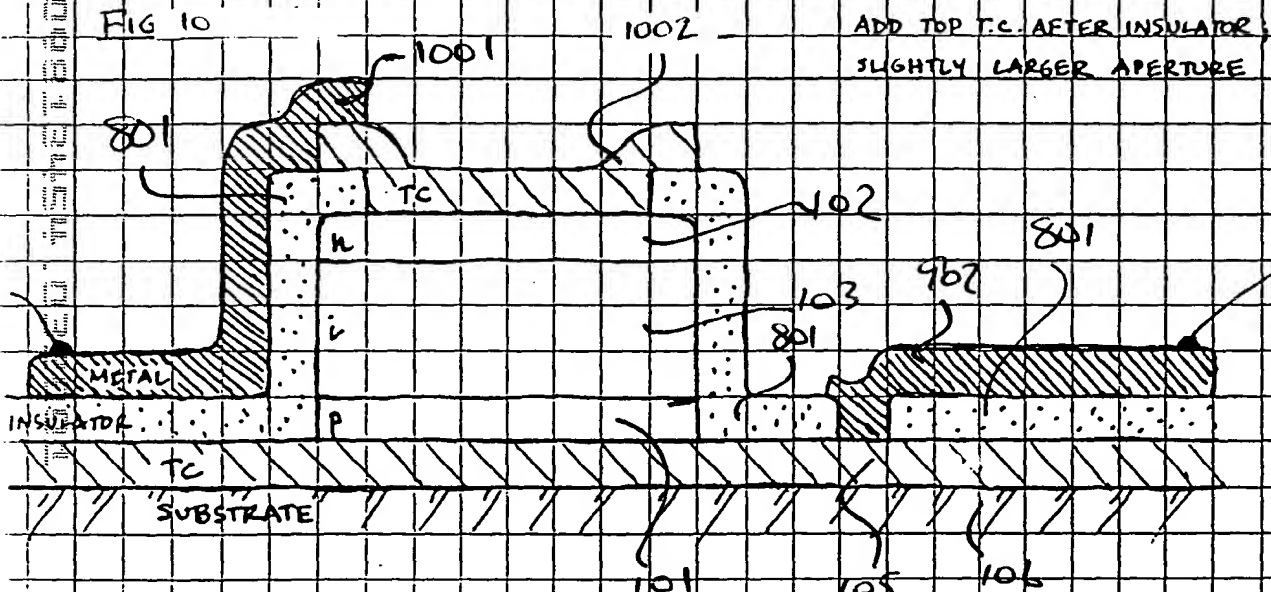


FIG 9



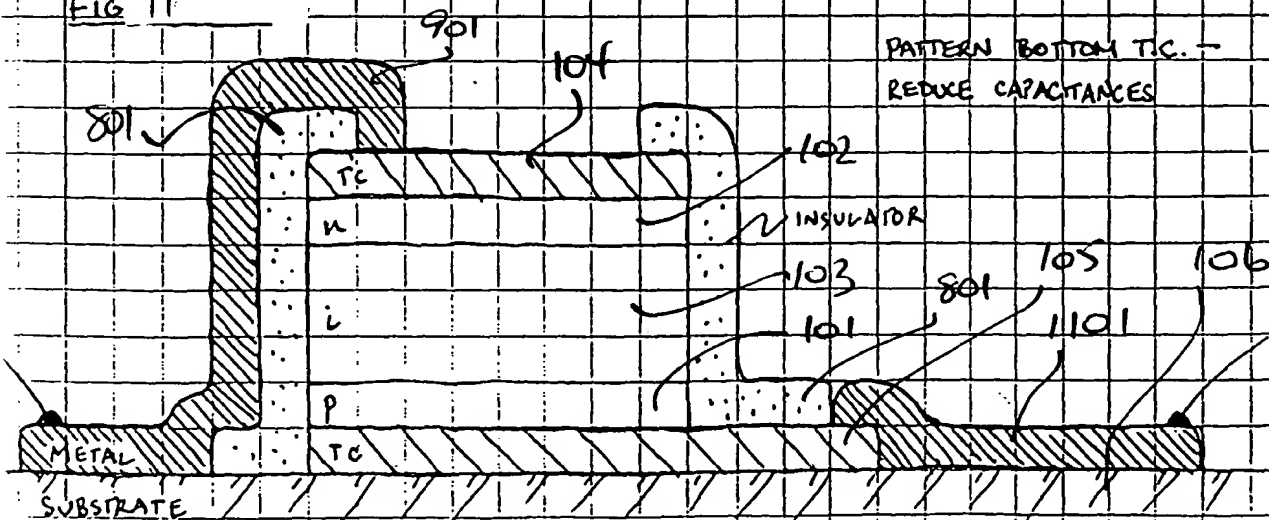
MOST SIMPLE STRUCTURE
 • DON'T PATTERN BOTTOM T.C.
 • USE TOP T.C. AS PIN ETCH MASK

FIG 10



ADD TOP T.C. AFTER INSULATOR
 SLIGHTLY LARGER APERTURE

FIG 11



PATTERN BOTTOM T.C. -
 REDUCE CAPACITANCES

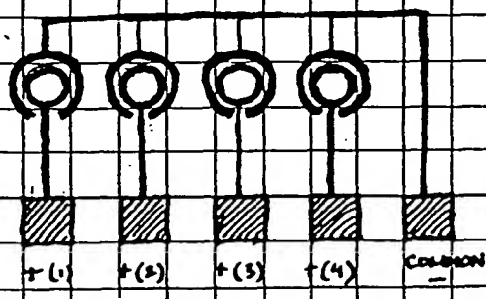
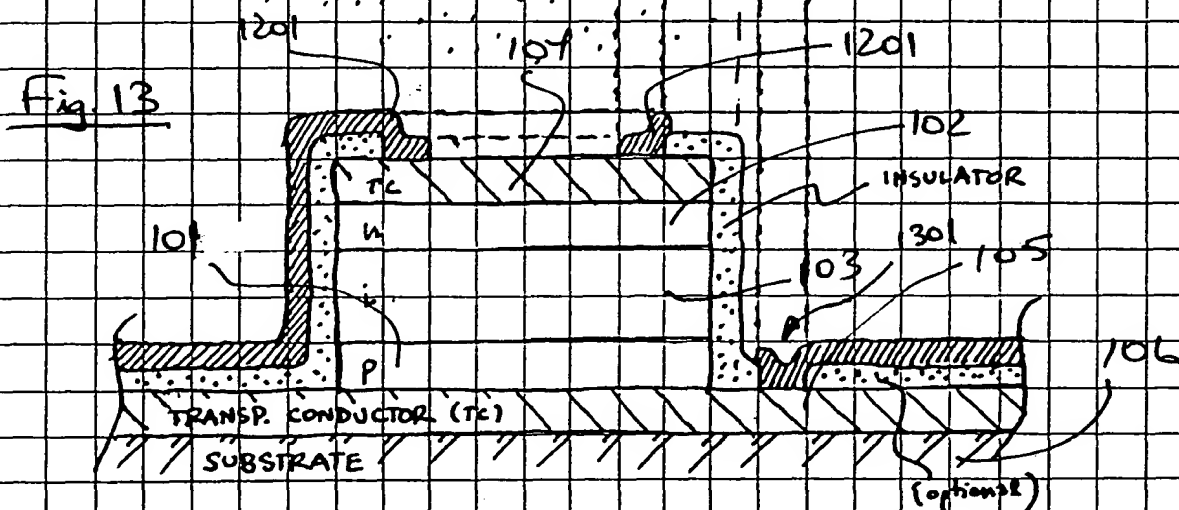
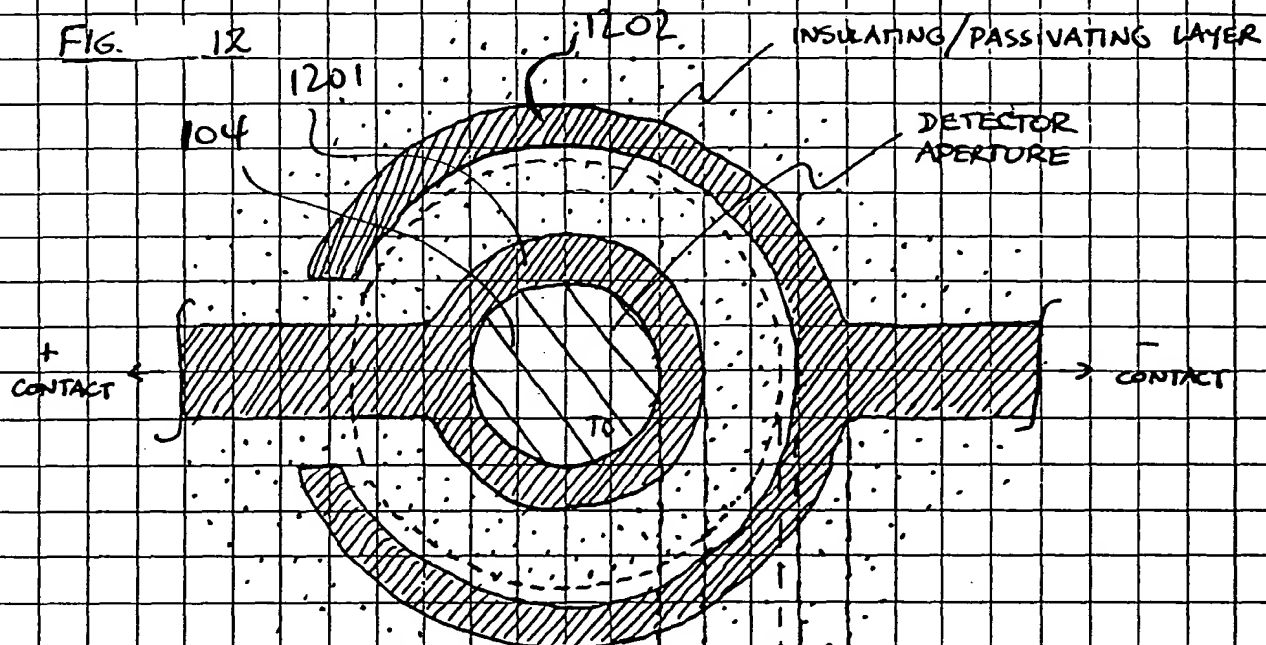


Fig. 14

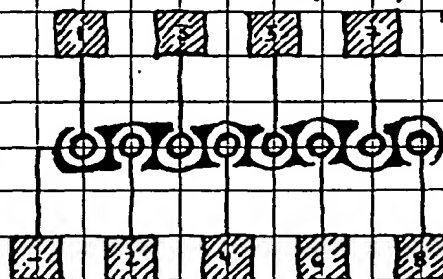


Fig. 15

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Fig. 16

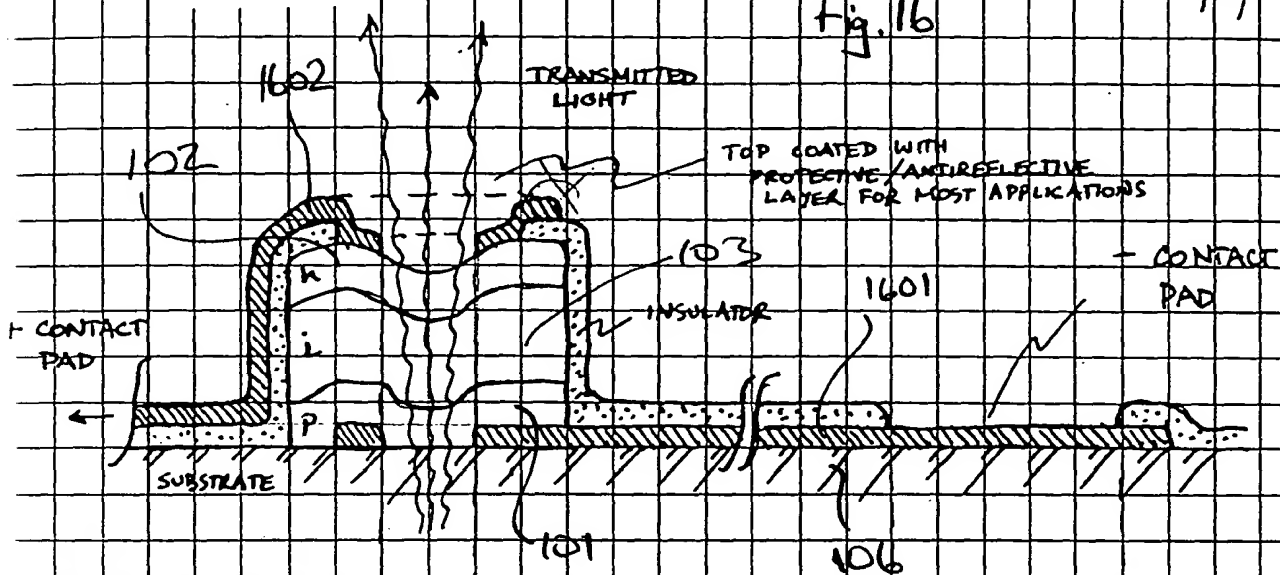
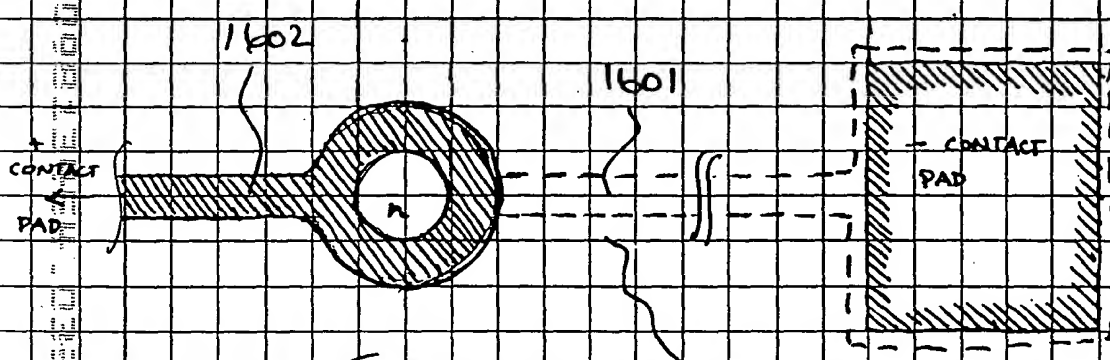


Fig. 17



BOTTOM METAL CONTACT MAY BE USED TO TIE TOGETHER ENTIRE ARRAY

Fig. 18

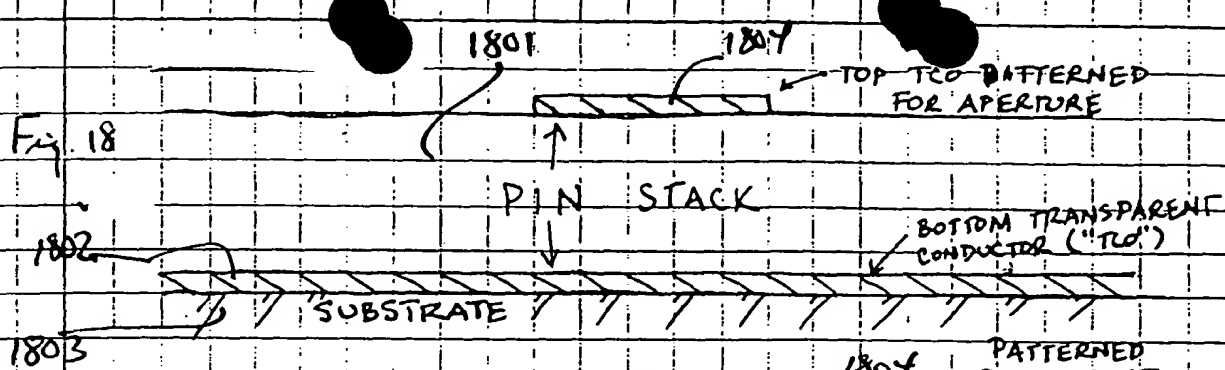


Fig. 19

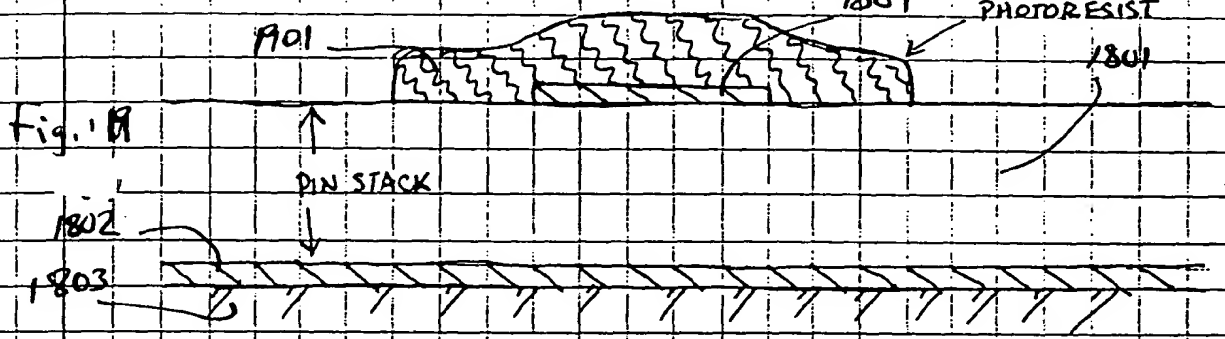


Fig. 20

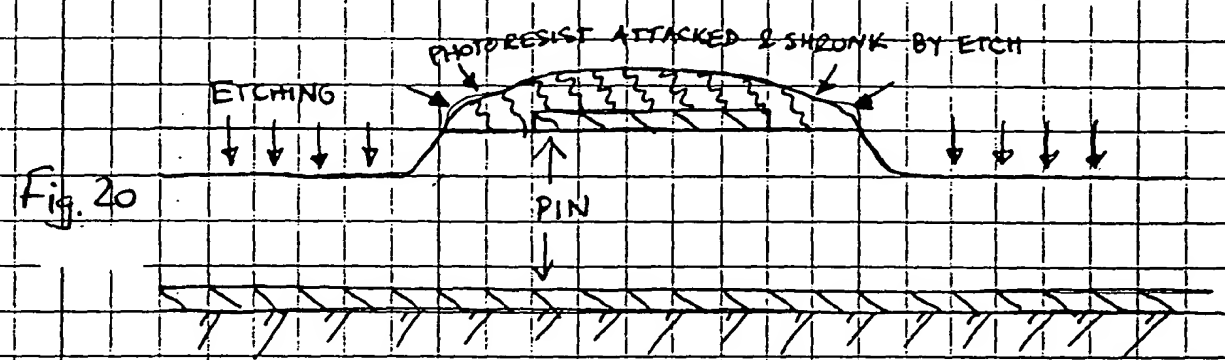


Fig. 21

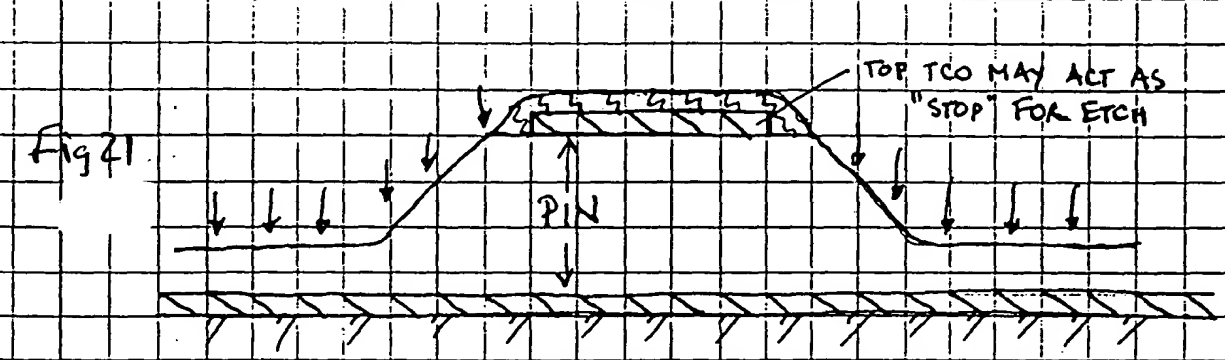
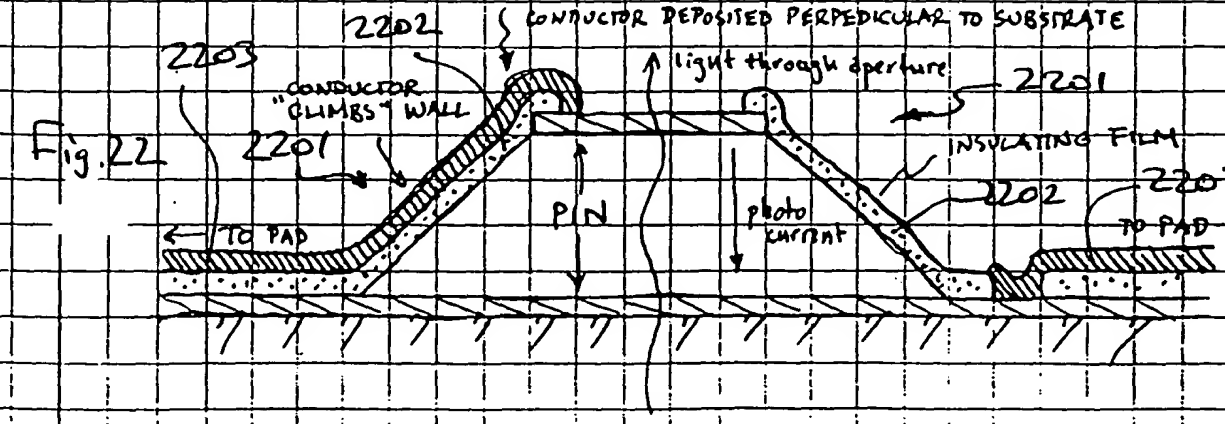
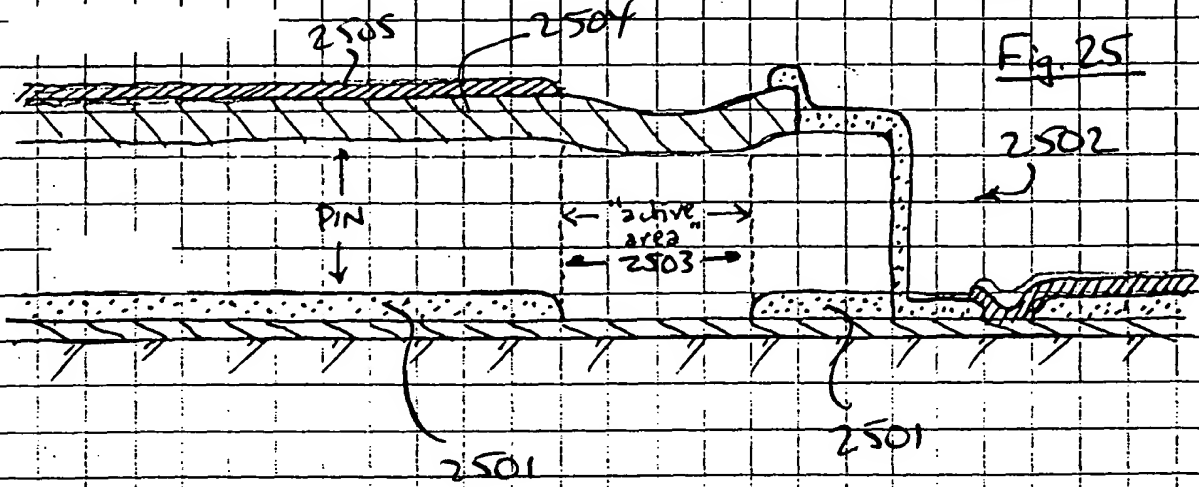
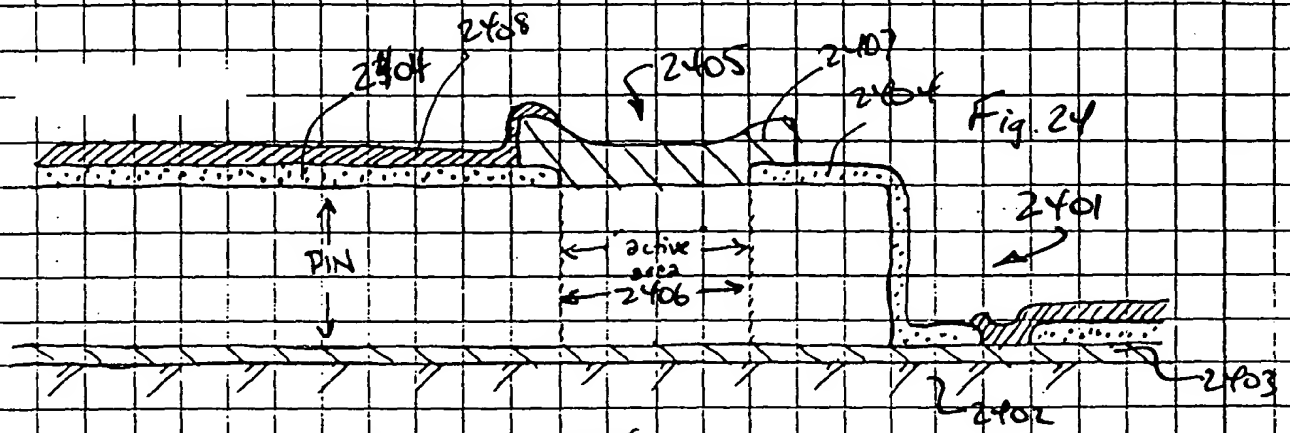
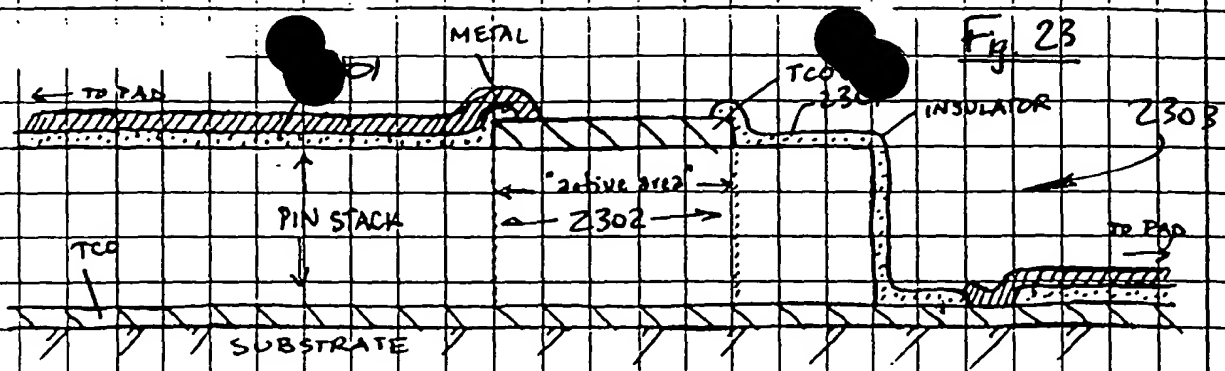


Fig. 22





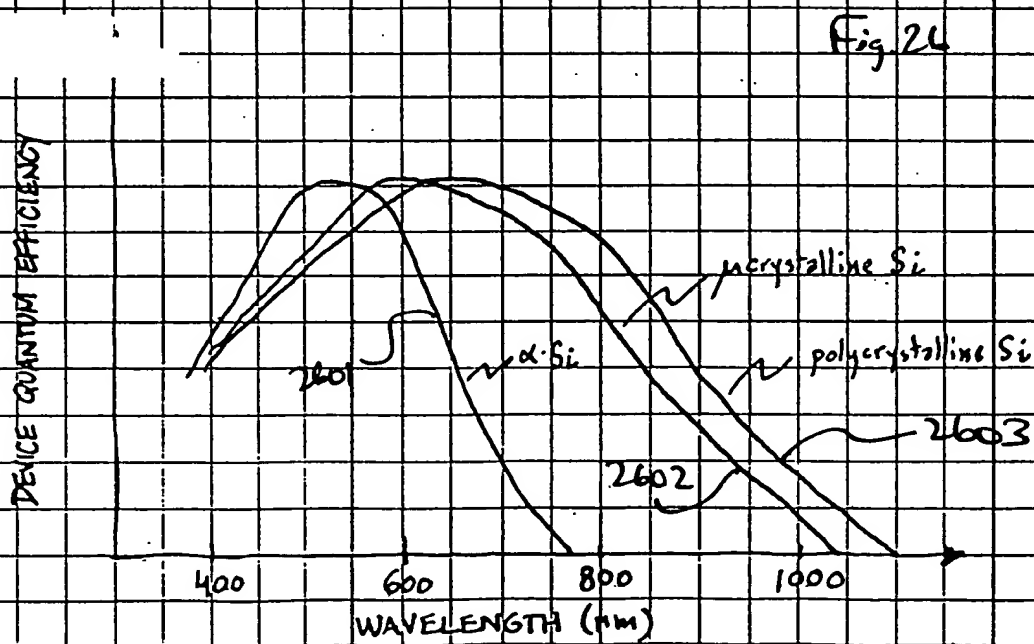


Fig. 27

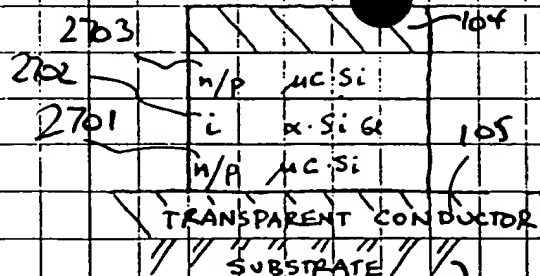


Fig. 28

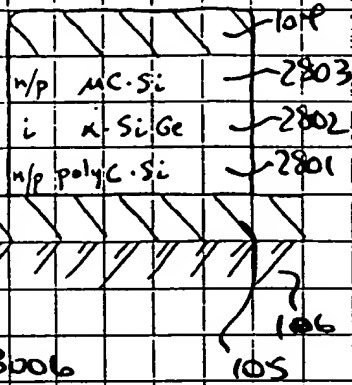


Fig. 29

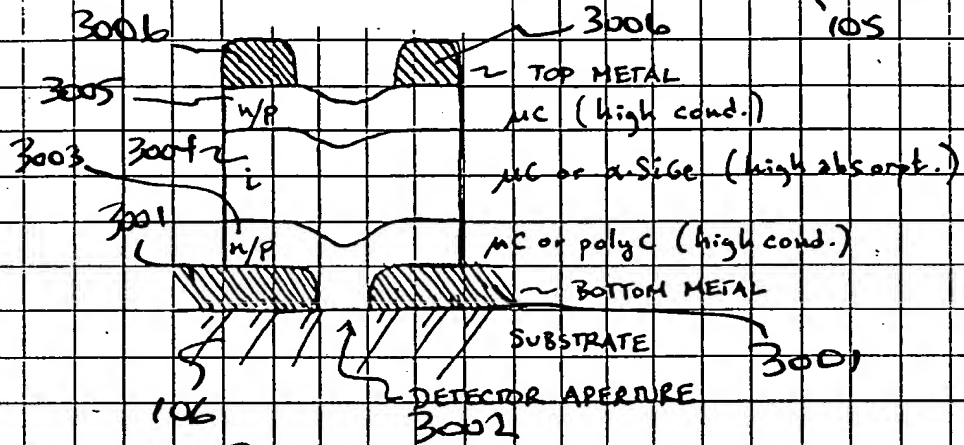
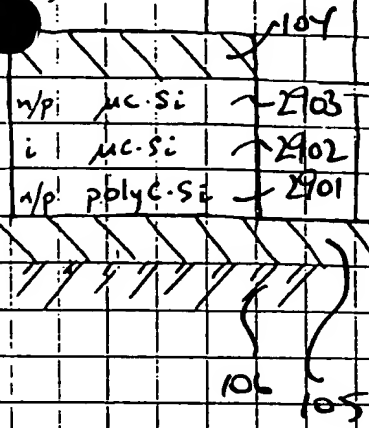


Fig. 30

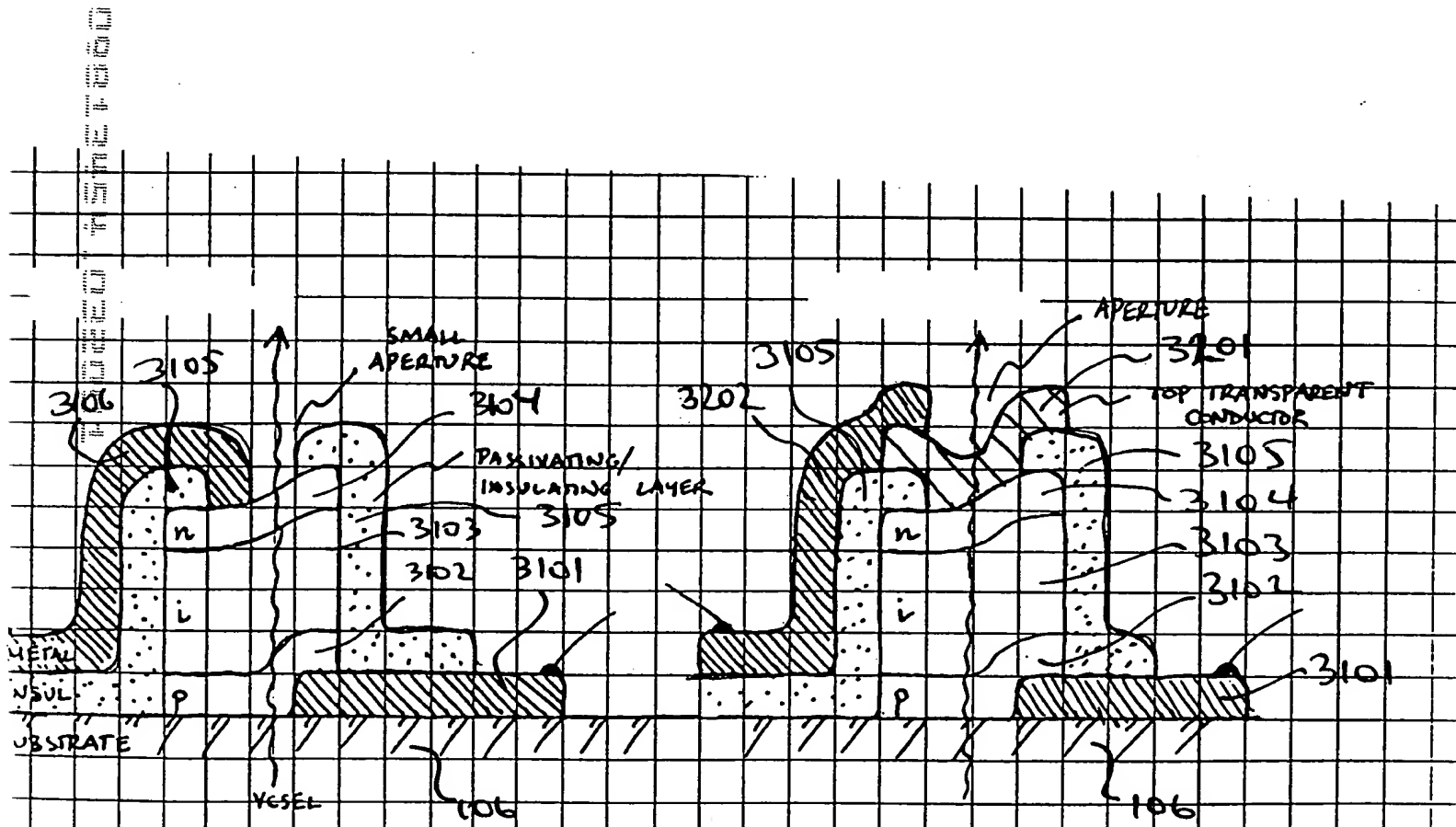
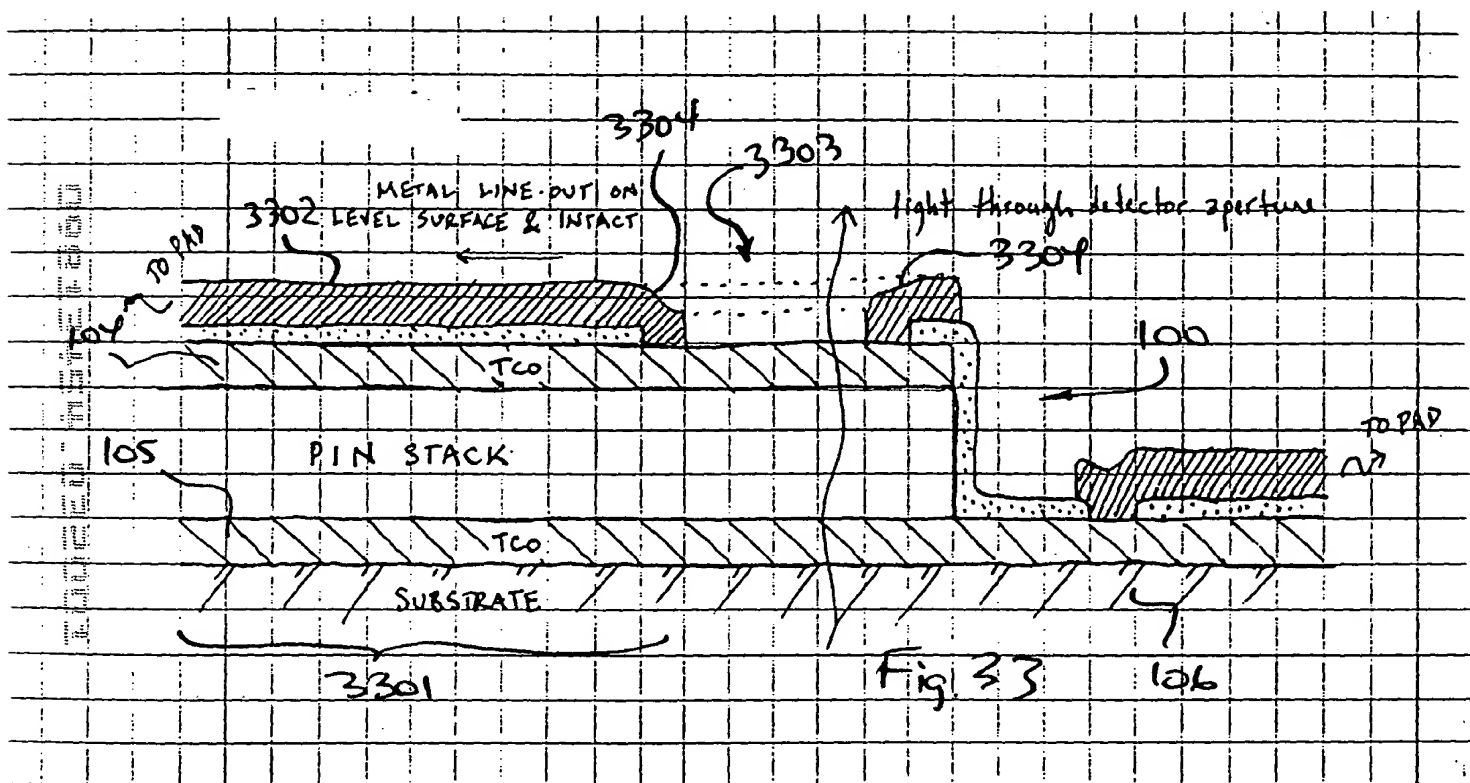
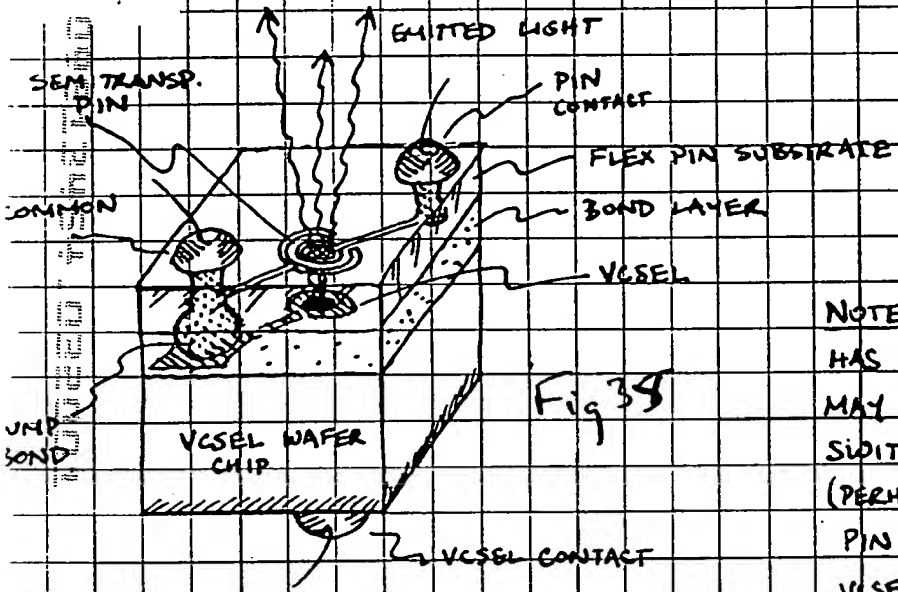
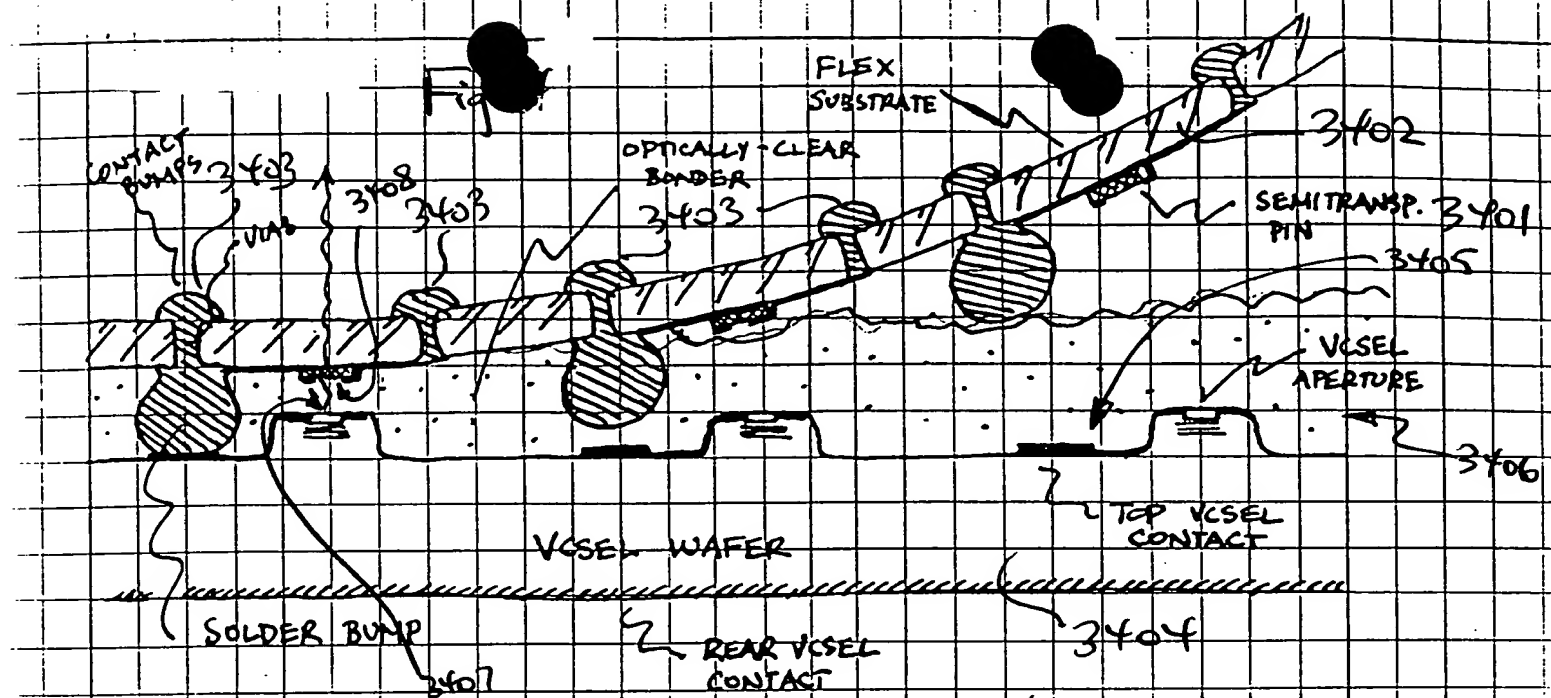


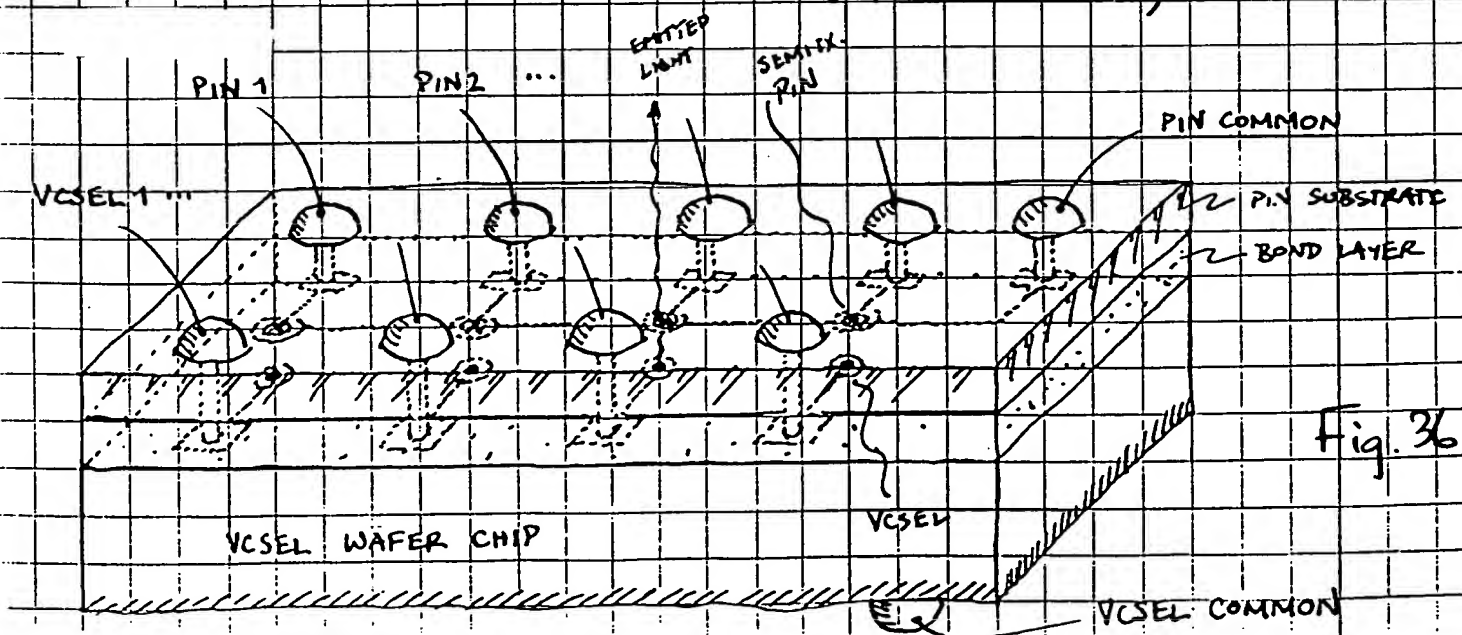
Fig 31

Fig 32





NOTE: ALTERNATIVE CONFIGURATION HAS 3 TOP CONTACTS (NO COMMON); MAY BE PREFERABLE FOR HIGH-SPD. SWITCHING. (PERHAPS EVEN FORM HOLE THROUGH PIN SUBSTRATE & BOND LAYER TO VCSEL TOP CONTACT).



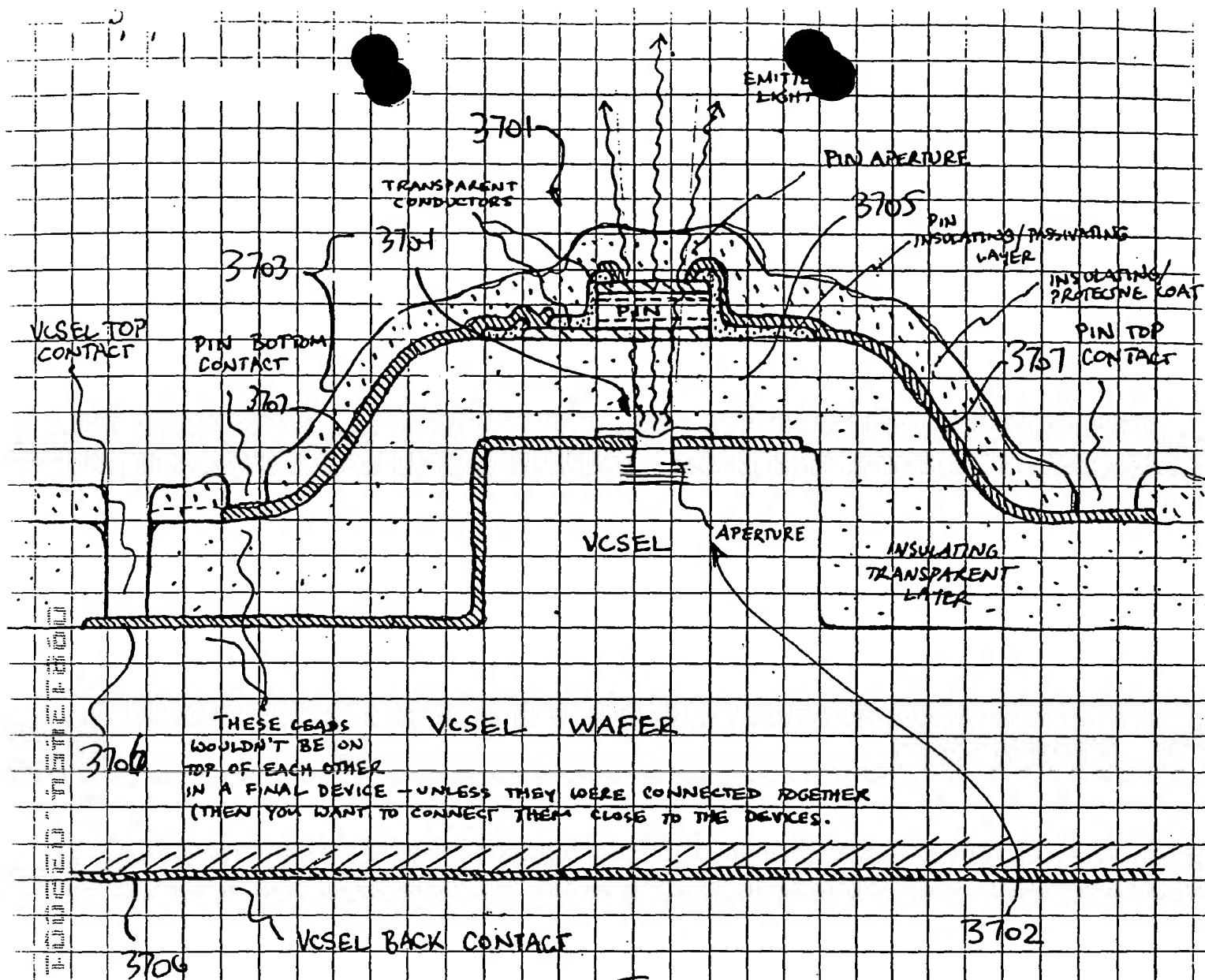


Fig. 37

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COLLAPSE LAYERS TO PROVIDE SHORTEST
VCSEL → FIBER PATH (no optics!)

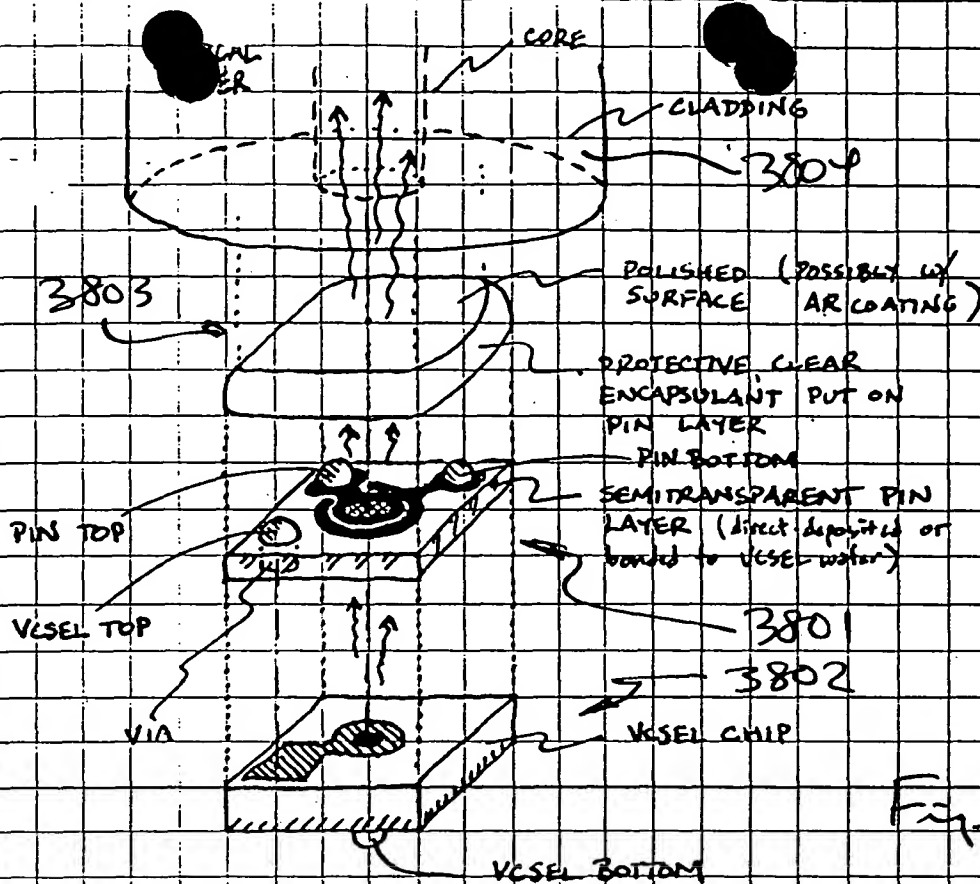


Fig. 38

.. SUCH A PACKAGE WOULD ALLOW LOW-COST, DIRECT COUPLING
IN A FIBER CONNECTOR (VCSEL APERTURE $\leq 25\mu\text{m}$ AND MULTIMODE
FIBER CORE $\approx 50-62.5\mu\text{m}$; VCSEL BEAM DIVERGENCE $\leq 20^\circ$, AND
PIN LAYER IS THIN).

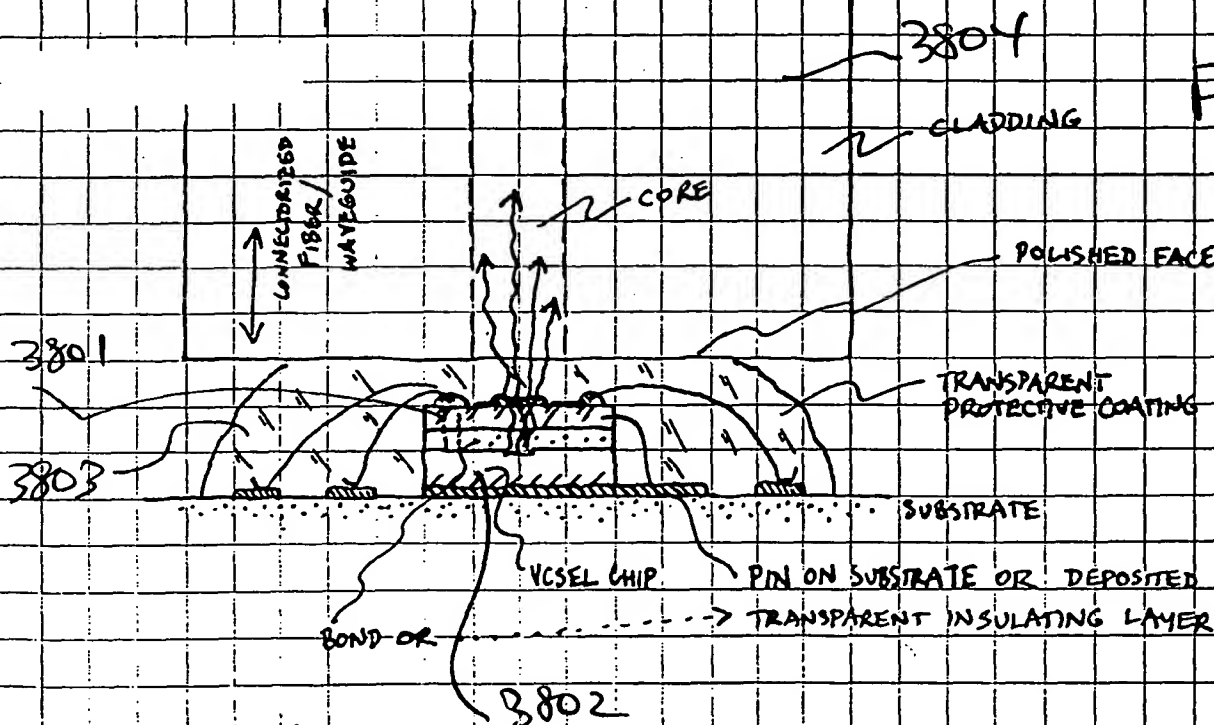
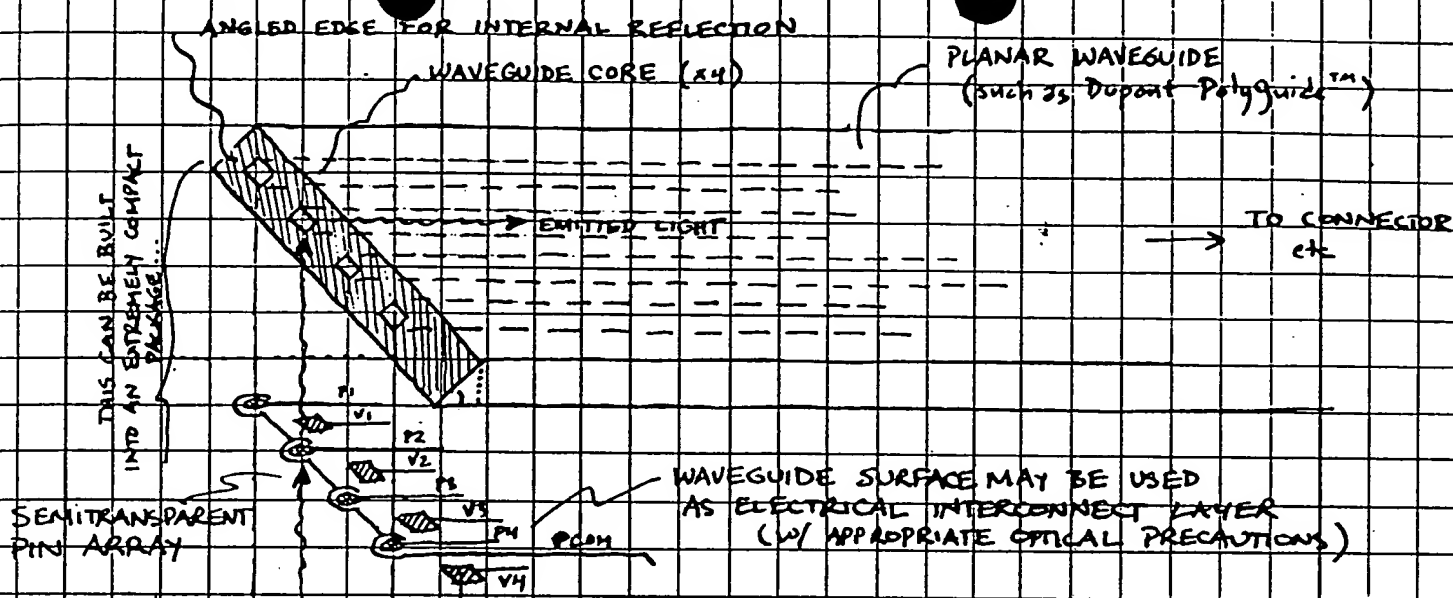


Fig. 39

Fig. 40



PIN ARRAY IS:

- (1) PATTERNED ON WAVEGD.
- (2) PATTERNED ON VCSEL CHIP
- OR (3) PATTERNED ON SEPERATE SUBSTRATE

Fig. 41

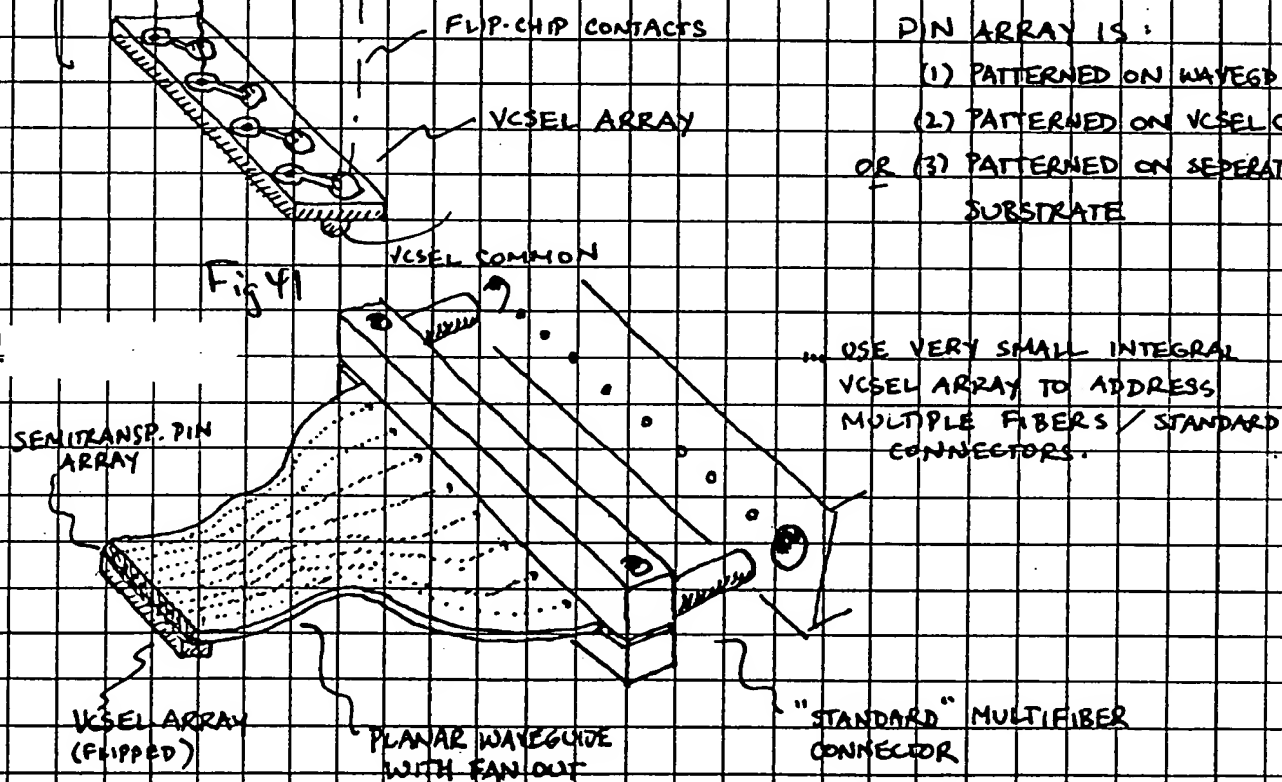


Fig. 42

